Examiner-Initiated Interview Summary	Application No.	Applicant(s)	
	09/923,604	HAPKE, FRIEDRICH	
	Examiner	Art Unit	
	John P. Trimmings	2138	

All Participants:

(1) *John P. Trimmings*.

(2) *Michael J. Ure*.

Status of Application: _____

(3) _____.

(4) _____.

Date of Interview: *11 July 2006*

Time: *4:00 pm*

Type of Interview:
- ☒ Telephonic
- ☐ Video Conference
- ☐ Personal (Copy given to: ☐ Applicant ☐ Applicant's representative)

Exhibit Shown or Demonstrated: ☐ Yes ☒ No
If Yes, provide a brief description:

Part I.

Rejection(s) discussed:
n/a

Claims discussed:
1-3

Prior art documents discussed:

Part II.

SUBSTANCE OF INTERVIEW DESCRIBING THE GENERAL NATURE OF WHAT WAS DISCUSSED:
See Continuation Sheet

Part III.

☒ It is not necessary for applicant to provide a separate record of the substance of the interview, since the interview directly resulted in the allowance of the application. The examiner will provide a written summary of the substance of the interview in the Notice of Allowability.

☐ It is not necessary for applicant to provide a separate record of the substance of the interview, since the interview did not result in resolution of all issues. A brief summary by the examiner appears in Part II above.

(Examiner/SPE Signature)

(Applicant/Applicant's Representative Signature – if appropriate)

Continuation of Substance of Interview including description of the general nature of what was discussed:
The claims as recorded in the PTO database (eDAN) for the amendment submitted on 3/14/2004 should start on a separate page. Since the claims as amended on 3/14/2004 are non-compliant, the examiner wishes to clarify the record with a full claim listing. The examiner has therefore rewritten all claims 1-3 as they should appear in the patent publication, as follows:

Claim 1. An arrangement for testing an integrated circuit comprising a combinational logic system, and a test circuit, which arrangement performs a test of the behavior of the combinational logic system in comparison with test software which emulates the nominal behavior of the integrated circuit, the arrangement comprising:
two identical software models of the combinational logic system to be tested, in which a test sample is applied for test purposes to a first of these software models and whose output signals are coupled to a second of these software models;
wherein the test circuit, in a test mode, applies a first test sample in a first test clock cycle to the input of the combinational logic system of the integrated circuit and receives the output signal in a buffer memory, and which feeds back this output signal as a second test sample in a second test clock cycle to the input of the combinational logic system and again receives the output signal of the combinational logic system in the buffer memory
wherein, at the end of the second test clock cycle, the arrangement compares the results of the combinational logic system of the integrated circuit in the buffer memory with the results of the second software model.

Claim 2. The arrangement as claimed in claim 1, characterized in that the buffer memory is constituted as a shift register by means of which the test samples are read and/or written.

Claim 3. A method of testing an integrated circuit comprising a combinational logic system, and a test circuit, in which method the behavior of the combinational logic system is compared with test software which emulates the nominal behavior of the integrated circuit, the method comprising:
providing two identical software models of the combinational logic system to be tested, in which a test sample is applied for test purposes to a first of these software models and whose output signals are coupled to a second of these software models;
wherein the test circuit, in a test mode, applies a first test sample in a first test clock cycle to the input of the combinational logic system of the integrated circuit and receives the output signal in a buffer memory and which feeds back this output signal as a second test sample in a second test clock cycle to the input of the combinational logic system and again receives the output signal of the combinational logic system in the buffer memory
wherein, at the end of the second test clock cycle, the arrangement compares the results of the combinational logic system of the integrated circuit in the buffer memory with the results of the second software model.

John P Trimmings
Examiner